

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet

1

of

2

Application Number

Complete if Known

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Filing Date

11/24/03

First Named Inventor

Correale, Jr. et al.

Art Unit

2819

Examiner Name

D. Chang

Attorney Docket Number

YOR920030373US1

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

Examiner Signature	<i>James D. O'Connell</i>	Date Considered	3/8/05
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Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number <u>18720 466</u>	
				Filing Date <u>11/24/03</u>	
				First Named Inventor <u>Correale, Jr. et al.</u>	
				Art Unit <u>2819</u>	
				Examiner Name <u>D. Chang</u>	
(use as many sheets as necessary)				Attorney Docket Number <u>YOR920030359US1</u>	
Sheet	2	of	2		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JC		LACKEY ET AL., Managing power and performance for System-on-Chip designs using Voltage Islands, Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design, 11/11/2002, Page(s) 195-202	
JC		USAMI ET AL., CLUSTERED VOLTAGE SCALING TECHNIQUES FOR LOW-POWER DESIGN, International Symposium on Low-Power Electronic Design, 4/1/1995, Page(s) 3-8, Publisher: ACM Press	
JC		USAMI ET AL., AUTOMATED LOW-POWER TECHNIQUE EXPLOITING MULTIPLE SUPPLY VOLTAGES APPLIED TO A MEDIA PROCESSOR, IEEE Journal of Solid-State Circuits, 3/1/1998, Page(s) 463-472, Volume 33, Number 3	
JC		YEH ET AL., LAYOUT TECHNIQUES SUPPORTING THE USE OF DUAL SUPPLY VOLTAGES FOR CELL-BASED DESIGNS, Proc. ACM/IEEE Design Auto. Conf., 6/1/1999, Page(s) 62-67	

Examiner Signature <u>D. Chang</u>	Date Considered <u>3/8/05</u>
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